IN THE CLAIMS

Please cancel Claims 1-11, 28-39, 43-46, and 49-59 without prejudice, and amend Claims 12, 18, 23, 40, 47, 48, and 60 as follows:

12. An integrated circuit, fabricated using the method comprising:

creating a customized description language model of an integrated circuit design by:

editing a first file specific to [a desired integrated circuit] said design;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information; and

running said script to create [a] said customized description language model [of said integrated circuit design];

generating a netlist which is descriptive of the circuitry of said integrated circuit;

compiling said netlist and said hardware description model to produce a compiled integrated circuit design;

fabricating at least one mask representing said compiled integrated circuit design; and

fabricating said integrated circuit using said at least one mask;

wherein said act of creating is performed at a high level of abstraction.

18. An apparatus adapted to generate integrated circuit designs, comprising;

a processor capable of running a computer program;

a storage device operatively coupled to said processor, said storage device being capable of storing at least a portion of a computer program;

an input device, operatively coupled to said processor, capable of receiving input from a user and transmitting said input to said processor; and

a computer program resident at least in part on said storage device, said computer program adapted to receive said input relating to a constrained set of design variables from said user and perform the following acts based on said input:

editing a first file specific to said integrated circuit design;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information; and

running said script to create said description language model of said integrated circuit design.

23. A system adapted for interactively generating an integrated circuit design at a high level of abstraction based on inputs received from a user, comprising:

a computer having a processor and an input device; and

a computer program capable of running on said processor, said computer program comprising:

a first algorithm having a plurality of user-selectable files, said user-selectable files comprising;

a first file comprising at least one instruction;

a second file comprising a plurality of cache configurations; and

a third file comprising a plurality of memory interface configurations;

a second algorithm capable of generating a script based on selections made by said user from said first, second, and third files and input to said computer program via said input device; and

a third algorithm capable of running said script to generate a description language model of said integrated circuit design.

40. A system for generating integrated circuit designs at a high level of abstraction, comprising:

a processor;

a storage device in data communication with said processor, said storage device being capable of storing and retrieving a computer program; and

a computer program stored within said storage device and adapted to run on said processor, said computer program comprising;

a user-configurable macro-instruction having at least a first user-selectable element, said first-selectable element being selected from the group comprising;

(i) a plurality of custom instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

a first algorithm capable of generating a script based on selections made by a user from said at least first user selectable element; and

a second algorithm capable of running said script to generate a description language model of an integrated circuit design.

47. A method of generating the design of an integrated circuit [using] rendered in a hardware description language, said method being performed at a high level of abstraction and comprising the acts of:

selecting a process technology;

editing a first file specific to the design, said act of editing comprising selecting at least one user-configurable parameter selected from the group comprising;

(i) processor instructions;

(ii) cache configuration;

(iii) memory interface configuration; and

(iv) system architecture configuration;

defining the location of at least one library file;

generating a script using said first file and said library;

running said script to create a customized hardware description language model of the design; and

running a synthesis algorithm to synthesize a file descriptive of said design.

48. A system for generating integrated circuit designs at a high level of abstraction, comprising:

means for processing digital data;

means for data storage in data communication with said processor means, said means for data storage being capable of storing and retrieving a computer program; and

a computer program stored within said means for data storage and adapted to run on said processor means, said computer program comprising;

means for selecting a process technology;

a user-configurable macro-instruction having at least one user-selectable element, said user-selectable element being selected from the group comprising;

(i) a plurality of instructions;

(ii) a plurality of cache configurations;

(iii) a plurality of memory interface configurations; and

(iv) a plurality of system architecture configurations;

means for generating a script based on said user selectable element and said process technology; and

means for running said script to generate a description language model of an integrated circuit design.

60. A method of designing a configurable processor, the method comprising:

generating, at a high level of abstraction, a processor specification having a user-definable portion, the user-definable portion of said specification including at least one user-defined instruction having a function associated therewith; and

based on said processor specification, generating a description of a hardware implementation of said configurable processor.

Please add the following new claims:

75. A method of generating the design of an integrated circuit at a high level of abstraction using a description language, comprising the acts of:

providing an existing processor core configuration;

editing a first file specific to the design, said editing comprising selecting a constrained set of input parameters associated with said configuration, said parameters comprising:

(i) at least one custom instruction;

(ii) a cache configuration; and

(iii) a memory interface configuration;

providing at least one library file;

generating a script using said first file, said library file, and user input information;

running said script to create a customized description language model; and

synthesizing said design based on said description language model.

76. A method of generating an integrated circuit design at a high level of abstraction, comprising:

providing a user with a plurality of optional instructions, including the ability to generate a customized instruction;

selecting at least one of said plurality of optional instructions;

selecting at least one cache configuration;

defining at least one memory interface;

generating a script based on said at least one optional instruction, cache configuration, and memory interface; and

running said script to generate a hardware description language model of said integrated circuit design.

77. A description language model of an integrated circuit design generated at a high level of abstraction using the method comprising:

editing a first file specific to said integrated circuit design including selecting a plurality of input parameters associated with said design, said parameters comprising:

(i) at least one custom instruction set; and

(ii) a cache configuration;

defining the location of at least one library file;

generating a script using said first file, said library file, and user input information; and

running said script to create said description language model of said integrated circuit design;

wherein said method is performed at a high level of abstraction.

78. A method of generating an extended processor design at a high level of abstraction, comprising:

providing the user with a basecase processor core configuration having a base instruction set;

providing a user with a plurality of optional instructions adaptable for use with said basecase core;

selecting at least one of said plurality of optional instructions;

selecting at least one cache configuration;

generating a script based on said at least one optional instruction, cache configuration, and basecase core; and

running said script to generate a hardware description language model of said processor design;

wherein said plurality of optional instructions and cache configurations are constrained so as to ensure the functionality of said processor design irrespective of the user's selections.

REMARKS

Claims 1-74 were pending in the application. By this paper, Applicant has cancelled Claims 1-11, 28-39, 43-46, and 49-59 without prejudice, amended Claims 12, 18, 23, 40, 47, 48, and 60, and added new Claims 75-78. Hence Claims 12-27, 40-42, 47-48, and 60-78 are now pending in the application.

Applicant has also by this paper amended the "Field of the Invention" portion of the specification to make it more descriptive of the actual invention. Applicant submits that the foregoing amendments add no new matter.

Interview

Applicant wishes to thank the Examiner for the courtesy of the personal interview on February 6, 2003.

Rejections under 35 U.S.C. §102

By this paper, Applicant has cancelled all claims rejected by the Examiner under 35 U.S.C. §102, thereby rendering all such rejections moot.